WHAT IS CLAIMED IS:

1. A random access memory, comprising:

a first circuit configured to receive a strobe signal and provide pulses in response to transitions in the strobe signal; and

a second circuit configured to receive the strobe signal to latch data into the second circuit, and to receive the pulses to latch the latched data into the second circuit after the transitions in the strobe signal.

2. The random access memory of claim 1, wherein the first circuit comprises:

an enable circuit configured to provide an enable signal; and

a buffer circuit configured to receive the strobe signal and the enable signal and provide the pulses in response to the enable signal and the strobe signal.

3. The random access memory of claim 2, wherein the enable circuit is configured to receive the pulses from the buffer circuit and stop providing the enable signal to the buffer circuit in response to receiving the pulses.

4. The random access memory of claim 1, wherein the first circuit provides one of the pulses during each cycle of the strobe signal and each cycle of a clock signal.

5. The random access memory of claim 1, wherein the second circuit comprises:

a first latch configured to latch first data at first transitions in the strobe signal; and

second latches configured to latch the latched first data from the first latch and second data at second transitions in the strobe signal.

6. The random access memory of claim 5, wherein the second circuit comprises:

third latches configured to latch in the latched first and second data from the second latches with the pulses after the second transitions.

7. The random access memory of claim 1, wherein the memory comprises a double data rate-I synchronous dynamic random access memory.

8. The random access memory of claim 1, wherein the memory comprises a double data rate-II synchronous dynamic random access memory.

9. A random access memory comprising:

a control circuit configured to receive a strobe signal and generate a pulse after one edge of the strobe signal and before the next edge of the strobe signal for each cycle of a clock signal.

10. The random access memory of claim 9, comprising a latch circuit configured to receive the strobe signal and the pulse, wherein the latch circuit is configured to latch data signals into the latch circuit with the strobe signal and to receive the pulse to prevent post-amble noise on the strobe signal from latching other signals into the latch circuit.

11. The random access memory of claim 9, wherein the control circuit comprises a delay chain configured to receive the clock signal.

12. The random access memory of claim 11, wherein the control circuit comprises a logic circuit configured to receive the strobe signal and an inverted clock signal.

13. The random access memory of claim 12, wherein the control circuit comprises a latch configured to receive a delay chain output signal from the delay chain and an output signal from the logic circuit.

14. The random access memory of claim 13, wherein the control circuit comprises a NOR gate configured to receive the strobe signal and a latch output signal from the latch.

15. A random access memory comprising:

a signal generation circuit comprising:

an enable controller configured to provide an enable signal; and

a controlled buffer configured to receive the enable signal and a strobe signal, wherein the enable controller and the controlled buffer are configured to generate a pulse at one edge of the strobe signal for each cycle of a clock signal; and

a plurality of latching circuits, wherein each latching circuit is configured to receive the strobe signal to latch data into the latching circuit and the pulse to block noise on the strobe signal from latching data into the latching circuit.

16. The random access memory of claim 15, wherein each latching circuit in the plurality of latching circuits comprises a first latching stage, a second latching stage and a third latching stage.

17. The random access memory of claim 16, wherein the pulse latches data into the third latching stage.

18. The random access memory of claim 16, wherein the first latching stage and the second latching stage are configured to receive the strobe signal to latch data into the first latching stage and the second latching stage.

19. A random access memory comprising:

a plurality of signal generation circuits, wherein each signal generation circuit comprises:

an enable controller configured to provide an enable signal; and

a controlled buffer configured to receive the enable signal and a strobe signal, wherein the enable controller and the controlled buffer are configured to generate a pulse at one edge of the strobe signal for each cycle of a clock signal; and

a plurality of latching circuits, wherein each latching circuit is configured to receive the pulse from one signal generation circuit in the plurality of signal generation circuits to block noise on the strobe signal from latching data into the latching circuit.

20. The random access memory of claim 19, wherein each latching circuit in the plurality of latching circuits comprises a first latching stage, a second latching stage and a third latching stage.

21. The random access memory of claim 20, wherein the pulse latches data into the third latching stage.

22. The random access memory of claim 20, wherein the first latching stage and the second latching stage are configured to receive the strobe signal to latch data into the first latching stage and the second latching stage.

23. A random access memory, comprising:

means for generating a pulse after a transition in a data strobe signal;

means for latching data using the data strobe signal; and

means for latching the latched data using the pulse.

24. The random access memory of claim 23, wherein the means for generating a pulse comprises a means for generating the pulse after a falling edge of the data strobe signal and before a rising edge of the data strobe signal.

25. The random access memory of claim 23, wherein the means for latching data comprises:

means for latching data at a rising edge of the data strobe signal;

means for latching data at a falling edge of the data strobe signal; and

means for latching latched data with the data strobe signal.

26. The random access memory of claim 23, wherein the means for latching the latched data comprises a third latch stage configured to receive the pulse and latch the latched data into the third latch stage.

27. A method for rejecting post-amble noise on a data strobe signal in a random access memory, comprising:

generating a pulse before the data strobe signal floats; and

latching data into a latch stage with the pulse to preserve the data.

28. The method of claim 27, wherein generating the pulse comprises generating the pulse during each cycle of the data strobe signal and each cycle of a clock signal.

29. The method of claim 27, wherein generating the pulse comprises generating the pulse after a falling edge of the data strobe signal.

30. The method of claim 27, wherein generating the pulse comprises:

generating an enable signal; and

generating a start of the pulse based on the enable signal and the data strobe signal.

31. The method of claim 27, wherein generating the pulse comprises:

receiving a signal at an enable circuit;

generating an enable signal from a transition on the received signal;

receiving the enable signal and the data strobe signal at a buffer circuit;

generating a start of the pulse based on the received enable signal and the received data strobe signal; and

receiving the start of the pulse at the enable circuit.